Patent claims

1. Fabrication method for a semiconductor structure having a partly filled trench, having the following steps:
provision of a semiconductor structure (1, 5) having a trench (2);
filling of the trench (2) with a filling (10) in such a way that the filling (10) projects above a surface (OF) of the semiconductor structure (1, 5) by a first height (h1), the filling (10) covering the trench (2) and the periphery (20) of the trench (2);
planarization of the filling (10) in a first etching step in such a way that the filling (10) is essentially planar with the surface (OF) of the semiconductor structure (1, 5); and
sinking of the filling (10) in the trench (2) in a second etching step by a predetermined depth (T) proceeding from the surface of the semiconductor structure (1, 5);
essentially the same plasma power and the same etchant composition being used for the first and second etching steps.

2. Method according to claim 1,
characterized
in that a planarization of the filling (10) is carried out in a zeroth etching step before the first etching step in such a way that the filling (10) projects above the surface (OF) of the semiconductor structure (1, 5) by a second height (h2), the filling (10) covering the trench (2) and the periphery (20) of the trench (2), the zeroth etching step having a higher etching rate than the first etching step.

3. Method according to claim 2,
characterized

in that essentially the same etchant composition as for the first and second etching steps but an increased plasma power are used for the zeroth etching step.

4. Method according to claim 1, 2 or 3, characterized in that at least the first etching step is carried out with a first time duration which is determined by an end point identification.

5. Method according to claim 2, 3 or 4, characterized in that the zeroth etching step and the second etching step are carried out with a predetermined zeroth and second time duration.

6. Method according to one of the preceding claims 1 to 4, characterized in that the second etching step is carried out with a second time duration which is determined by an end point identification.

7. Method according to one of the preceding claims, characterized in that the etchant composition contains SF_6, Ar and Cl_2.

8. Method according to one of the preceding claims, characterized in that the semiconductor structure (1, 5) comprises a semiconductor substrate (1) and a mask (5) situated thereon, the mask (5) being used for the etching of the trench (2).

9. Method according to one of the preceding claims 4 to 8, characterized

in that the end point identification is carried out by interferometry.